AMENDMENTS

In accordance with 37 CFR §1.121, please amend the above-identified application as set forth below.

Amendments to the Specification

1. Please amend the specification by inserting the replacement paragraphs below.

[0017] In one aspect of the present invention VBI data is reinserted into a DVB bitstream by creating a gray scale palette in an OSD data area or memory, sizing a VBI data area, locating a VBI area and optionally storing both in an OSD data storage area or other memory associated with it. Alternatively this data may be regenerated upon demand. The information is used by the OSD for generating a VBI luma waveform bitmap. The OSD overlays the VBI luma waveform bitmap onto an uncompressed digital video signal for display output.

[0023] Referring now to the figures in which like reference numerals indicate like elements, figure 1 is a block diagram of a typical integrated receiver/decoder unit (IRD) 10. The IRD 10 receives a radio frequency input comprising a standardized digital video broadcast bitstream according to the MPEG protocol from satellite dish 20. Components within the IRD 10, all which are in operative communication with one another, include the control processor 30, tuner 32, RAM 34, packet identification filters 36, ~~buffer 38,~~ MPEG decoder 40, digital analog converter 42, buffer 44, Universal Asynchronous

Receiver/Transmitter (UART) ~~UART~~ 46, a link to an Ethernet or LAN 48, and an operator interface comprised of a LCD display 50 and ~~a keyboard~~ panel buttons 52. The digital analog converter outputs a signal comprising video, audio or other data to display devices such as a television or speakers (not shown). The operation of a typical IRD 10 is more fully described in US Patent Applications No. 10/350,930 and 10/400,972 incorporated by reference herein.

[0024] Figure 2 discloses some of the components within the control processor 30 ~~50~~. The control processor 30 ~~50~~ may be configured in a variety of ways. A separate microprocessor 110 may work in conjunction with a video decoder chip 120, or a single ASIC may include both functions as separate modules. In either case a memory region is dedicated to OSD.

[0026] The OSD memory region 130 is configurable to include multiple OSD memory regions 132 dedicated to various tasks. Within each OSD memory region dedicated to inserting VBI data, a portion will be configured for storing information locating the VBI display according to an XY position 134. A single pixel among the horizontal array of pixels, 720 in NTSC format, is identified as the beginning X position. Similarly one of the lines in the vertical array is identified as the starting Y position. Memory region 132 will also have a horizontal and vertical size 136 configured. Size is defined by a number of pixels (horizontal length) by a number of lines (vertical height). These positions and

dimensions are largely hardware specific. ~~A 256-byte~~ An eight bit gray scale palette 138 is also stored ~~at 138~~ in the memory region 132. Finally, a memory component for the actual bitmap data 140 is configured and associated with the palette and position and size data. The bitmap data is received from the VBI waveform builder module 112 and temporarily stored in the bitmap data region 140.

[0029] A palette is a lookup table. Different memory regions may each have their own palette, as in the depicted embodiment, or each memory region may alternatively refer to a palette stored in a different memory region. Palettes may be configured for different ranges of color. For example, if two ~~bytes~~ bits are allocated per pixel, four colors are available. If ~~eight bytes~~ four bits are allocated per pixel, sixteen colors are available. If eight ~~bytes~~ bits are allocated per pixel, 256 colors are available. Different palette sizes may be used within the scope of the present invention according to available memory capacity and speed requirements. In the depicted embodiment, eight ~~bytes~~ bits are used per pixel.